Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently amended) A universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer;

a shift register coupled to said FIFO buffer;

a serial transmission line coupled to said shift register for connecting to a remote processor;

a circuit for detecting a last word transmitted from said FIFO buffer over said serial transmission line;

a transmitter empty circuit for generating ~~a transmitter empty signal~~ a control signal relating to the availability of said serial transmission line on a ~~transmitter empty~~ control line when a last word transmitted from said FIFO buffer is detected;

a delay circuit for delaying generation of said ~~transmitter empty~~ control signal for a programmable delay time; and

a programmable register for setting said programmable delay time.

2. (Currently amended) The UART of claim 1 wherein said ~~transmitter empty~~ control signal is ~~an internal signal~~ triggered from a stop bit of said last word.

3. (Previously presented) The UART of claim 1 wherein said programmable register comprises a shadow register which is a write-only register with the same address as a read-only register only read by a user.

4. (Currently amended) The UART of claim 3 wherein said write-only register comprises the first [[4]] four bits of a modem status register.

5. (Original) The UART of claim 1 wherein said programmable register is a four bit register.

6. (Currently amended) The UART of claim 1 further comprising:

a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and

said delay circuit and said programmable register being a single circuit and register connected to control the delay of said ~~transmitter empty~~ control signal for each of said channels.

7. (Currently amended) A universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer;

a shift register coupled to said FIFO buffer;

a serial transmission line, coupled to said shift register for connecting to a remote processor;

a circuit for detecting a last word transmitted from said ~~FIFO buffer~~ shift register over said serial transmission line;

a transmitter empty circuit for generating ~~a transmitter empty~~ an RTS signal on ~~a transmitter empty~~ an RTS control line when a last word transmitted from said ~~FIFO buffer~~ shift register is detected, wherein said ~~transmitter empty~~ RTS signal is ~~an internal signal~~ triggered from a stop bit of said last word;

a delay circuit for delaying generation of said ~~transmitter empty~~ RTS signal for a programmable delay time;

a programmable register for setting said programmable delay time, wherein said programmable register comprises a shadow register which is a write-only register with the same address as a read-only register only read by a user;

a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and

said delay circuit and said programmable register being a single circuit and register connected to control the delay of said ~~transmitter empty~~ RTS signal for each of said channels.

8. (Currently amended) The UART of claim 7 wherein said write-only register comprises the first [[4]] four bits of a modem status register.

9. (Previously presented) The UART of claim 7 wherein said programmable register is a four bit register.

10. (Currently amended) The UART of claim 7 further comprising at least [[8]] eight of said channels.

11. (New) The UART of claim 2 wherein said stop bit is detected in said shift register.

12. (New) The UART of claim 1 wherein said control signal is an RTS signal.

13. (New) A universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer;

a shift register coupled to said FIFO buffer;

a serial transmission line, coupled to said shift register for connecting to a remote processor;

a circuit for detecting a last word transmitted from said shift register over said serial transmission line;

a transmitter empty circuit for generating a control signal relating to the availability of said serial transmission line on a control line when a last word transmitted from said shift register is detected;

a delay circuit for delaying generation of said control signal for a programmable delay time; and

a programmable register for setting said programmable delay time.